

363	65	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

RE38140

RE38140

## U.S. REISSUE Patent Application

O.I.P.# 12W 103 SCANNED G.A. GW	O.G. PUBLICATION DATE 4-17-2001	REISSUE PATENT DATE JUN 10 2003
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APPLICATION NO. 09/781120	CONT/PRIOR D	CLASS 363✓	SUBCLASS 65	ART UNIT 2838	EXAMINER Berkey
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Gregory Schaffer

PARENT FILE  
OF REISSUE  
APPLICATION  
10/409,538

Dual interleaved DC to DC switching circuits realized in an integrated circuit

PTO-2  
12/8

☒ SURRENDER OF ORIGINAL PATENT EB (Exr. Initials) 5,810,216 ORIGINAL PATENT NUMBER

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b> Sheets Drawn: <u>4</u> Figs. Drawn: <u>5</u> Print Figs.: <u>2d</u>		<b>CLAIMS ALLOWED</b> Total Claims: <u>63</u> Print Claim for O.G.: <u>22</u>	
	<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.		<b>NOTICE OF ALLOWANCE MAILED</b> <u>12/12/02</u>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	Agent: <u>Concetta Barbone</u> <b>Primary Examiner</b> <u>POJ Balazs</u> 6/02 (Primary Examiner) (Date)		<b>ISSUE FEE</b> Amount Due: <u>1280</u> Date Paid: <u>12-18-02</u>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<b>FINAL SPRE REVIEW</b> <u>POJ 12/14/02</u> (INITIALS)		<b>ISSUE BATCH NUMBER</b>	

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